

REMARKS/ARGUMENTS

Claims 1-21 are pending. The independent claims have been amended. No new matter has been added.

Claims 1, 2, 8, 9, 14-16, and 21) were rejected under 35 U.S.C. Section 103 for allegedly being obvious in view of Zhao (U.S. Pat. No. 6,002,406) and Kacevas et al. (U.S. Pat. No. 6,429,873).

Claims 3, 10, and 17 were rejected under 35 U.S.C. Section 103 for allegedly being obvious in view of Zhao, Kacevas et al., and Baldwin (U.S. Pat. No. 6,650,333).

Claims 4-6, 11-13, and 18-20 were rejected under 35 U.S.C. Section 103 for allegedly being obvious in view of Zhao, Kacevas et al., Baldwin, and Merz et al. (U.S. Pat. No. 4,692,880).

The undersigned is grateful for the examiner's time and attention during an interview conducted March 21, 2006. A discussion of the claims and the cited references was made, although no agreement was reached.

Zhao was relied on for generally disclosing the recited determining an amount of storage for a level of detail (LOD) other than the base image. However, a review of Zhao including the examiner's cited portions do not reveal determining an amount of storage for storing a level of detail. For example, the Abstract mentions "storing a data representative of an object in various LODs;" however, there is no discussion of computing an amount of storage. The Abstract also mentions that with their technique "the amount of memory required for storing the LOD data is also minimized." Again, this does not disclose computing an amount of storage. Col. 3, lines 4-7, also cited in the Office action, discloses similar matter as in the Abstract. Zhao therefore provides no teaching relating to the recited subject matter.

Claim 1 recites in part, identifying a size of an immediately larger LOD. Kacevas was cited at column 1, lines 24-35 for showing this limitation. However, this cited portion describes starting with the largest version and constructing progressively lower resolution representations. This does not show or suggest the recited identifying a size of an immediately

larger level of detail; Kacevas “start with the largest version,” so there is no “immediately larger level of detail.”

Claim 1 recites in part, calculating the amount of storage to be used for storing the first level of detail. Column 1, lines 24-35 was cited for showing this limitation. However, this cited portion describes constructing lower resolution representations. Kacevas does not discuss a step of calculating the amount of storage for storing the LOD.

During the interview, the examiner pointed to column 3, lines 23-25, and suggested that the calculation of *Vsize* might be a teaching of the recited calculating the amount of storage to be used for storing the first level of detail. Column 4, lines 39-64 also discuss the use of *Vsize*. However, Kacevas describes *Vsize* as being “the vertical size of LOD 0.” *Col. 3, line 24*. The vertical size is used to compute coordinates of LODs. See for example, the discussion from column 3, line 31-51. It is earnestly submitted that a vertical size is not the same as the recited amount of storage for storing an LOD.

Kacevas is concerned with computing address locations; i.e., locations in memory, not amount of memory for storing LODs. The title of the Kacevas reference is “addressing of monolithic texture maps.” Kacevas teaches placing related maps of a mip-map at memory locations so that only the base address of the mip-map needs to be maintained. *Col. 2, lines 4-7*. Kacevas provides an example of address computation from column 3, line 12 to column 4, line 17. Fig. 2 shows a logic circuit for determining the location of a selected map beginning at column 4, line 39.

Zhao, as discussed above does not teach or suggest calculating amount of storage for a LOD. Kacevas does not teach or suggest the recited limitations as discussed above. The Section 103 rejection of claim 1 is therefore overcome, since the references taken in combination do not show or suggest all of the recited elements.

Independent claims 8 and 15 recite similar limitations and thus are patentable over the cited art for at least the same reasons set forth above.

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PATENT

CONCLUSION

In view of the foregoing, Applicants believe all claims now pending in this Application are in condition for allowance and an action to that end is respectfully requested.

If the Examiner believes a telephone conference would expedite prosecution of this application, please telephone the undersigned at 650-326-2400.

Respectfully submitted,


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